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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,734	07/24/2003	Naoto Fujishima	1639.1008D	8062
21171	7590	12/10/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,734	FUJISHIMA, NAOTO	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 July 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1 and 2 is/are rejected.

7) Claim(s) 3 and 4 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 24 July 2003 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. 10/156,757.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 07/24/03.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation as recited in dependent claims 3 and 4 “wherein the etching back of the first conductor includes over-etching the first conductor so that only a portion of the first conductor lower than the surface of the semiconductor substrate remains un-removed” must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

The Information Disclosure Statement filed on July 24th, 2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujishima et al. (U.S. Patent 6,316,807).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

In re claim 1, Fujishima discloses a method for manufacturing a semiconductor device, comprising:

forming a trench 71 in a surface region of a semiconductor substrate 62, of a first conductivity type (p-type) (col. 7, lines 6-17 and FIG. 8);

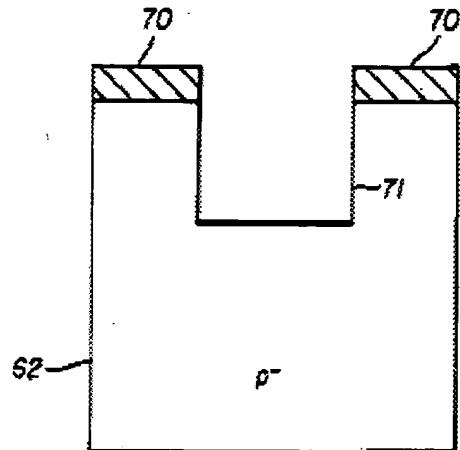


FIG. 8

forming a drift region, of a second conductivity type, around the trench (Abstract);
forming a gate insulating film 80, having a uniform thickness, along a side surface and a bottom surface of the trench and inside the trench and forming a first conductor 82 along a surface of the gate insulating film (col. 7, lines 19-31 and FIG. 13a),

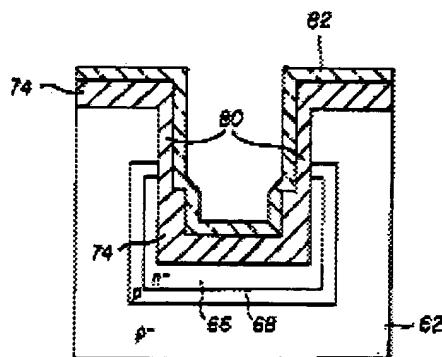


FIG. 13a

etching back the first conductor in an active region so that the first conductor remains only in side surface regions of the trench (col. 7, lines 32-57 and FIG. 15a);

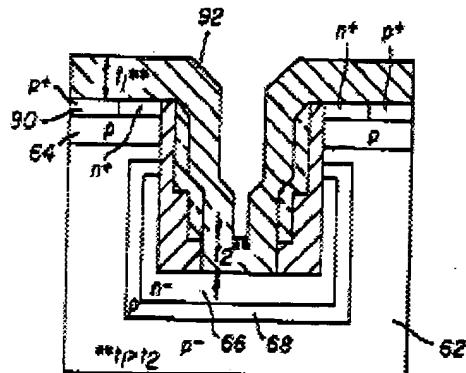


FIG. 15a

forming a base region (p-) of the first conductivity type (p-type), and a source region (n+), of the second conductivity type (n-type), in a surface region of the semiconductor substrate outside the trench (col. 7, lines 32-57 and FIG. 16b);

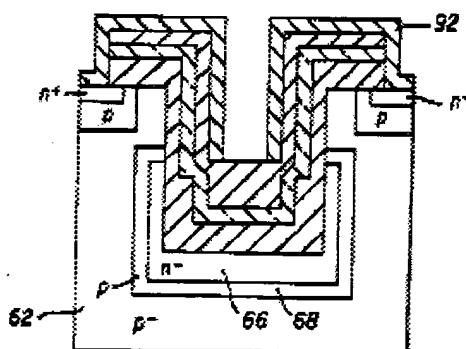


FIG. 16b

forming an interlayer dielectric 84 inside the first conductor (col. 7, lines 19-30 and FIG. 15b);

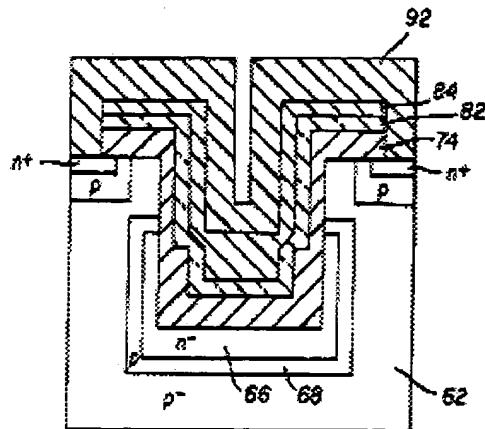


FIG. 15b

selectively removing a bottom of the interlayer dielectric in the active region; forming a drain region 58 of, the second conductivity type (n-type), at the bottom of the trench (col. 7, lines 32-57 and FIG. 16a); and

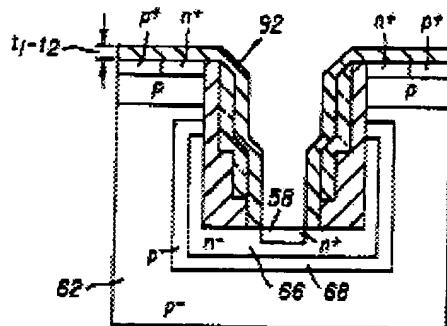


FIG. 16a

forming a second conductor 61 in the trench, the second conductor electrically connecting to the drain region (col. 7, lines 32-57 and FIG. 18a).

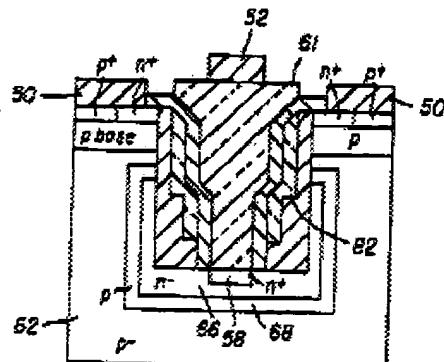


FIG. 18a

In re claim 2, Fujishima discloses that the method for manufacturing a semiconductor device of claim 1, further comprising: forming an interlayer dielectric 80 on a surface of the semiconductor substrate 62, opening contact holes through the interlayer dielectric (col. 7, lines 32-57), forming a gate electrode 54 that electrically connects to the first conductor 82, a drain electrode 52 that electrically connects to the second conductor 61, and a source electrode 50 that electrically connects to the source region (FIGS. 18a-b).

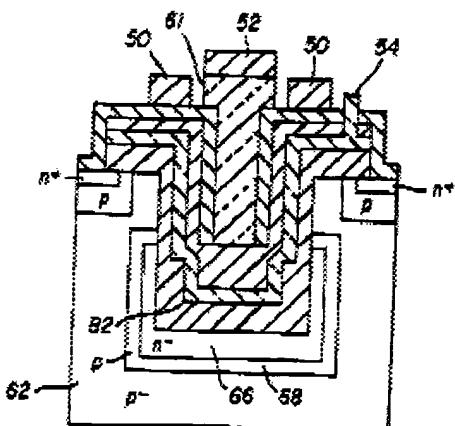


FIG. 18b

Allowable Subject Matter

Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 8th, 2004



**W. DAVID COLEMAN
PRIMARY EXAMINER**